UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,074	12/31/2001	Dong Suk Shin	P 282792 HD-1049	5615

909 7590 07/31/2003

PILLSBURY WINTHROP, LLP
P.O. BOX 10500
MCLEAN, VA 22102

EXAMINER
SONG, MATTHEW J

ART UNIT	PAPER NUMBER
1765	7

DATE MAILED: 07/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Files Copy

Office Action Summary	Application No.	Applicant(s)	
	10/032,074	SHIN, DONG SUK	
	Examiner	Art Unit	
	Matthew J Song	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dieumegard et al (US 5,090,932) in view of Gonzalez et al (US 6,194,746).

Dieumegard et al teaches a monocrystalline substrate of silicon **1** with an insulating layer of silica **2**, thereon (col 3, ln 30-67 and Figs 2a-2d). Diemegard et al also teaches windows are opened in the silica layer, this reads on applicant's opening a contact hole in the insulating layer, and selective epitaxy of silicon forms pyramidal peaks **4**, this reads on applicant's conical structure, on the bared zone of the substrate. Dieumegard et al also teaches the selective epitaxy of silicon can be done either at reduced pressure and at reduced pressure the optimum gas mixture may be formed by dichlorosilane, hydrogen and hydrochloric acid at a temperature ranging from 850-950°C (col 4, ln 1-67).

Dieumegard et al does not teach a polycrystalline or amorphous silicon portion fills the remainder of the contact hole.

In a method of forming a semiconductor device, note entire reference, Gonzalez et al teaches a nitride layer **108** and an oxide layer **104** deposited on a silicon wafer **95**. Gonzalez et al also teaches holes **110** are formed and extend through the nitride layer and the oxide layer (Fig 22). Gonzalez et al also teaches epitaxial depositing P-doped silicon in the exposed regions and

growing of epitaxial silicon is both time consuming and an expensive process. As such, it is preferable to minimize the thickness of the epitaxial silicon layer and a polysilicon layer **111** is deposited over the silicon wafer so as to fill the remaining portion of each hole **110**. Gonzalez et al also teaches forming the epitaxial silicon layer using LPCVD at a temperature of 950-1200°C in an atmosphere of silicon, SiH_2Cl_2 or silane (col 12, ln 50 to col 13, ln 30). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Dieumegard et al with Gonzalez et al's filling a hole with a minimal amount of epitaxial silicon and filling the rest of the hole with polysilicon to minimize the amount of epitaxial silicon which needs to be grown, thereby reducing cost and production time (col 13, ln 4-10).

3. Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dieumegard et al (US 5,090,932) in view of Gonzalez et al (US 6,194,746) as applied to claims 1 above, and further in view of Ang et al (US 6,319,783).

The combination of Dieumegard et al and Gonzalez et al teach all of the limitations of claim 2, as discussed previously including a reaction gas of silane or dichlorosilane, except the reaction gas is a gas mixture comprising MS and H_2 or a gas mixture comprising DSC and H_2 and a dopant gas is PH_3.

In a method of selective epitaxial growth, note entire reference, Ang et al teaches an epitaxial silicon layer is selectively grown on exposed regions of a semiconductor substrate via LPCVD at a temperature of 600-1000°C using silane or dischlorosilane as a source or using disilane and HCl as a source, with hydrogen as a carrier gas. Ang et al also teaches in situ doped regions are formed via the addition of phosphine (col 3, ln 25-67). It would have been obvious to

a person of ordinary skill in the art at the time of the invention to modify the combination of Dieumegard et al and Gonzalez et al with Ang et al's gas mixture to form a selective epitaxial silicon layer at a reduced temperature as low as 600°C, thereby reducing operating costs.

Referring to claim 3, the combination of Dieumegard et al, Gonzalez et al and Ang et al is silent to the flow rate of gases. Flow rates of gases is well known in the art to be a result effective variable, as evidenced by Cain (US 5,624,582) below. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Dieumegard et al, Gonzalez et al and Ang et al by optimizing the flow rate of gases by conducting routine experimentation of result effective variables.

Referring to claim 4, the combination of Dieumegard et al, Gonzalez et al and Ang et al teach in situ doping of an epitaxial silicon layer using phosphine (PH_3) ('783 col 3, ln 55-65). The combination of Dieumegard et al, Gonzalez et al and Ang et al is silent to the flow of PH_3 is controlled to obtain a phosphorous doping concentration between $1x10^{19}$ to 10^{21} atoms/cc. It is well known in the art to dope a silicon plug with a concentration of phoshpine to a concentration of $1x10^{19}$ to 10^{21} atoms/cc, as evidenced by Sung et al (US 6,180,453) below. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Dieumegard et al, Gonzalez et al and Ang et al by optimizing the flow rate to obtain a well-known concentration of a phosphine dopant in a silicon layer by conducting routine experimentation.

Referring to claim 5, the combination of Dieumegard et al, Gonzalez et al and Ang et al teach a LPCVD of epitaxial silicon. The combination of Dieumegard et al, Gonzalez et al and Ang et al is silent to the pressure in within a range of approximately 1-200 Torr. It is well known

in the art that LPCVD is performed at a medium vacuum within the claimed range, as evidenced by Cain (US 5,624,582) and Kessler et al (US 4,756,272). Also, pressure is well known in the art to be a result effective variable in a LPCVD process, as evidenced by Cain (US 5,624,582). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Dieumegard et al, Gonzalez et al and Ang et al by optimizing the pressure by conducting routine experimentation.

Referring to claim 3-5, the selection of reaction parameters such as temperature and concentration is obvious (In re Aller 105 USPQ 233, 255 (CCPA 1955)).

4. Claims 6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dieumegard et al (US 5,090,932) in view of Gonzalez et al (US 6,194,746) as applied to claims 1 above, and further in view of Lee (US 6,455,366).

The combination of Dieumegard et al and Gonzalez et al teach all the limitations of claim 6, as discussed previously, except applying a dry cleaning process, applying a wet cleaning process and baking the exposed portion of the silicon substrate in H_2 before selectively growing a silicon epitaxial layer in the contact hole.

In a method of forming a semiconductor device, note entire reference, Lee teaches a doped epitaxial silicon layer is selectively formed only at a portion in which a semiconductor substrate is exposed through low-pressure chemical vapor deposition. Lee also teaches before the epitaxial layer is formed a cleaning process is performed to remove an oxide film and cleaning the semiconductor substrate using RCA cleaning, UV ozone cleaning, HF dipping or a combination of these. The UV ozone cleaning reads on applicant's dry cleaning and the RCA

cleaning and HF dipping reads on applicant's wet cleaning. Lee also teaches before the doped epitaxial silicon layer is formed, the substrate is hydrogen baked at a temperature of 800-900°C for 1-5 minutes in situ (col 3, ln 10-50). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Dieumegard et al and Gonzalez et al with Lee's cleaning process of dry cleaning, wet cleaning and a hydrogen bake to remove an oxide film, which is well known in the art to be detrimental, on a substrate surface prior to selectively forming an epitaxial silicon layer.

Referring to claim 9, the combination of Dieumegard et al, Gonzalez et al and Lee teach a hydrogen bake at 800-900°C for 1-5 minutes (60-300 seconds). Overlapping ranges are held to be obvious (MPEP 2144.05).

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dieumegard et al (US 5,090,932) in view of Gonzalez et al (US 6,194,746) and Lee (US 6,455,366), as applied to claims 6 above, and further in view of Kawai (US 6,284,664).

The combination of Dieumegard et al, Gonzalez et al and Lee teach all of the limitations of claim 7, as discussed previously, except the dry cleaning process comprises treating the substrate using NF_3/O_2 plasma for approximately 20-30 seconds.

In a method of forming a semiconductor device, note entire reference, Kawai teaches contact holes formed in an interlayer oxide film laid on both a silicon substrate and wiring pattern. Kawai also teaches a step for eliminating an organic layer deposited at the bottom of the contact hole, through the use of cleaning gas plasma containing NF_3 and O_2. Kawai also teaches forming a conductive plug in the contact hole after removal of the organic layer (col 2, ln 45-65

and col 6, ln 30-40). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Dieumegard et al, Gonzalez et al and Lee with Kawai cleaning gas plasma of NF_3 and O_2 to remove a organic film, thereby improving resistance of the semiconductor device (col 4, ln 1-60).

Referring to claim 7, the combination of Dieumegard et al, Gonzalez et al, Lee and Kawai is silent to treating the substrate for 20 to 30 seconds. The duration of a plasma treatment process is well known in the art to be a result effective variable. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Dieumegard et al, Gonzalez et al, Lee and Kawai by optimizing the treating time by conducting routine experimentation of a result effective variable. The selection of reaction parameters such as temperature and concentration is obvious (In re Aller 105 USPQ 233, 255 (CCPA 1955)).

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dieumegard et al (US 5,090,932) in view of Gonzalez et al (US 6,194,746) and Lee (US 6,455,366), as applied to claims 6 above, and further in view of Clark et al (US 5,242,468).

The combination of Dieumegard et al, Gonzalez et al and Lee teach all of the limitations of claim 8, as discussed previously, except the wet cleaning process comprises treating using a mixed solution of BOE and H_2SO_4 for approximately 20-30 seconds.

In a method of treating semiconductor wafers with liquid cleaning agents, note entire reference, Clark et al teaches a wide variety of cleaning solutions in semiconductor manufacture at various stages in the manufacturing process and examples are HF, H_2SO_4 and various

combinations such as buffered oxide etch (col 4, ln 65 to col 5, ln 20). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Dieumegard et al, Gonzalez et al and Lee with Clark et al's solution of H_2SO_4 and BOE because substitution of known equivalents for the same purpose is held to be obvious. (MPEP 2144.06)

Referring to claim 8, the combination of Dieumegard et al, Gonzalez et al, Lee and Clark et al is silent to treating the substrate for 20 to 30 seconds. The duration of a wet chemical treatment process is well known in the art to be a result effective variable. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Dieumegard et al, Gonzalez et al, Lee and Clark et al by optimizing the treating time by conducting routine experimentation of a result effective variable. The selection of reaction parameters such as temperature and concentration is obvious (In re Aller 105 USPQ 233, 255 (CCPA 1955)).

7. Claims 10-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dieumegard et al (US 5,090,932) in view of Gonzalez et al (US 6,194,746) and Ang et al (US 6,319,783) as applied to claims 2-5 above, and further in view of Economikos et al (US 6,198,167).

The combination of Dieumegard et al, Gonzalez et al and Ang et al teach all of the limitations of claim 10, as discussed previously, except growing the polycrystalline or amorphous silicon portion at a temperature of approximately 550-650°C.

In a method of forming a semiconductor device, note entire reference, Economikos et al teaches an insulator layer having one or more vias whereby a portion of a epitaxial silicon

surface is exposed and depositing an amorphous silicon material layer on the exposed surface (col 2, ln 30-67). Economikos et al also teaches amorphous silicon is deposited using conventional low pressure chemical vapor deposition at a temperature of 500-560°C and a polycrystalline is deposited at temperatures greater than 560°C, typically of about 565-650°C (col 3, ln 5 to col 4, ln 10). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Dieumegard et al, Gonzalez et al and Ang et al with Economikos et al deposition temperature of amorphous and polycrystalline silicon to produce an expected result.

Referring to claim 10, the combination of Dieumegard et al, Gonzalez et al, Ang et al and Economikos et al teach the deposition SEG of silicon at 600-1000°C ('783 col 3, ln 50-60) and the deposition of amorphous or polycrystalline silicon at a temperature of 500-650°C ('167 col 3, ln 15 to col 4, ln 10). Overlapping ranges are held to be obvious (MPEP 2144.05).

Referring to claim 11, the combination of Dieumegard et al, Gonzalez et al, Ang et al and Economikos et al teach silane or dicholorosilane with a hydrogen carrier gas and phosphine for N-doped regions ('783 col 3, ln 55-60).

Referring to claim 12, note the arguments regarding claim 3, above.

Referring to claim 13, note the arguments regarding claim 4, above.

Referring to claim 14, note the arguments regarding claim 5, above.

Referring to claim 15, the combination of Dieumegard et al, Gonzalez et al, Ang et al and Economikos et al does not teach the thickness of the single crystal silicon portion has a height of approximately 500 angstroms. Gonzales et al teaches it is preferable to minimize the thickness of the epitaxial silicon layer. Therefore, it would have been obvious to a person of ordinary skill in

the art at the time of the invention to modify the combination of Dieumegard et al, Gonzalez et al, Ang et al and Economikos et al by optimizing the thickness of the layer by conducting routine experimentation of a result effective variable. The selection of reaction parameters such as temperature and concentration is obvious (In re Aller 105 USPQ 233, 255 (CCPA 1955)).

Referring to claim 16, the combination of Dieumegard et al, Gonzalez et al, Ang et al and Economikos et al does not teach the step of growing the single crystal silicon portion is completed in approximately 30-60 seconds. Time is a well known process variable in the vapor deposition process. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Dieumegard et al, Gonzalez et al, Ang et al and Economikos et al by optimizing the time to obtain same by conducting routine experimentation of a result effective variable. The selection of reaction parameters such as temperature and concentration is obvious (In re Aller 105 USPQ 233, 255 (CCPA 1955)).

Referring to claim 17, note arguments regarding claim 10.

8. Claims 18 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dieumegard et al (US 5,090,932) in view of Gonzalez et al (US 6,194,746), Ang et al (US 6,319,783) and Economikos et al (US 6,198,167), as applied to claims 10-17 above, and further in view of Lee (US 6,455,366).

The combination of Dieumegard et al, Gonzalez et al, Ang et al and Economikos et al teach all the limitations of claim 18, as discussed previously, except applying a dry cleaning process, applying a wet cleaning process and baking the exposed portion of the silicon substrate in H_2 before selectively growing a silicon epitaxial layer in the contact hole.

In a method of forming a semiconductor device, note entire reference, Lee teaches a doped epitaxial silicon layer is selectively formed only at a portion in which a semiconductor substrate is exposed through low pressure chemical vapor deposition. Lee also teaches before the epitaxial layer is formed a cleaning process is performed to remove an oxide film and cleaning the semiconductor substrate using RCA cleaning, UV ozone cleaning, HF dipping or a combination of these. The UV ozone cleaning reads on applicant's dry cleaning and the RCA cleaning and HF dipping reads on applicant's wet cleaning. Lee also teaches before the doped epitaxial silicon layer is formed, the substrate is hydrogen baked at a temperature of 800-900°C for 1-5 minutes in situ (col 3, ln 10-50). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Dieumegard et al, Gonzalez et al, Ang et al and Economikos et al with Lee's cleaning process of dry cleaning, wet cleaning and a hydrogen bake to remove an oxide film, which is well known in the art to be detrimental, on a substrate surface prior to selectively forming an epitaxial silicon layer.

Referring to claim 18, the combination of Dieumegard et al, Gonzalez et al, Ang et al, Economikos et al and Lee is silent to removing the substrate. This is inherent to the combination of Dieumegard et al, Gonzalez et al, Ang et al, Economikos et al and Lee because the device is required to be removed from the apparatus so it can be used.

Referring to claim 21, note the arguments regarding claim 9.

Referring to claim 22, the combination of Dieumegard et al, Gonzalez et al, Ang et al, Economikos et al and Lee teaches a epitaxial layer with a pyramidal structure and growing a second layer on the epitaxial layer and on a sidewall of the contact hole ('746 Fig 22 and col 13, ln 20-30).

9. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dieumegard et al (US 5,090,932) in view of Gonzalez et al (US 6,194,746), Ang et al (US 6,319,783) and Economikos et al (US 6,198,167) and Lee (US 6,455,366) as applied to claims 18 and 21-22 above, and further in view of Kawai (US 6,284,664).

The combination of Dieumegard et al, Gonzalez et al, Ang et al, Economikos et al and Lee teach all of the limitations of claim 19, as discussed previously, except the dry cleaning process comprises treating the substrate using NF_3/O_2 plasma for approximately 20-30 seconds.

In a method of forming a semiconductor device, note entire reference, Kawai teaches contact holes formed in an interlayer oxide film laid on both a silicon substrate and wiring pattern. Kawai also teaches a step for eliminating an organic layer deposited at the bottom of the contact hole, through the use of cleaning gas plasma containing NF_3 and O_2. Kawai also teaches forming a conductive plug in the contact hole after removal of the organic layer (col 2, ln 45-65 and col 6, ln 30-40). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify combination of Dieumegard et al, Gonzalez et al, Ang et al, Economikos et al and Lee with Kawai cleaning gas plasma of NF_3 and O_2 to remove a organic film, thereby improving resistance of the semiconductor device (col 4, ln 1-60).

Referring to claim 19, the time limitation has been held to be obvious, note the arguments regarding claim 7.

10. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dieumegard et al (US 5,090,932) in view of Gonzalez et al (US 6,194,746), Ang et al (US 6,319,783) and

Economikos et al (US 6,198,167) and Lee (US 6,455,366), as applied to claims 18 and 21-22 above, and further in view of Clark et al (US 5,242,468).

The combination of Dieumegard et al, Gonzalez et al, Ang et al, Economikos et al and Lee teach all of the limitations of claim 20, as discussed previously, except the wet cleaning process comprises treating using a mixed solution of BOE and H_2SO_4 for approximately 20-30 seconds.

In a method of treating semiconductor wafers with liquid cleaning agents, note entire reference, Clark et al teaches a wide variety of cleaning solutions in semiconductor manufacture at various stages in the manufacturing process and examples are HF, H_2SO_4 and various combinations such as buffered oxide etch (col 4, ln 65 to col 5, ln 20). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify combination of Dieumegard et al, Gonzalez et al, Ang et al, Economikos et al and Lee with Clark et al's solution of H_2SO_4 and BOE because substitution of known equivalents for the same purpose is held to be obvious. (MPEP 2144.06)

Referring to claim 20, the time limitation has been held to be obvious, note the arguments regarding claim 8.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Cain (US 5,624,582) teaches deposition parameters used in LPCVD are gas composition, temperature, pressure and flow rate (col 10, ln 1-11) and LPCVD achieves a medium vacuum of several hundred millitorr to about 10 torr (col 9, ln 30-40).

Kessler et al (US 4,756,272) teaches pressure in a LPCVD chamber are typically 0.25 to 2 Torr with temperatures ranging between 300-700°C and gas flows between 100-1000 std. cm^3/min (col 1, ln 25-35).

Yoo et al (US 6,211,082) teaches source gas may employ a carrier gas for a smooth flow in a CVD process (col 3, ln 5-20).

Kang et al (US 6,197,683) teaches a source can be mixed with a carrier gas to provide a smooth gas flow into a deposition chamber in a CVD process (col 6, ln 9-35).

Sung et al (US 6,180,453) teaches a single crystalline silicon plug with a bulk concentration between 1E19-1E21 atoms/cm3 using a phosphine dopant (col 4, ln 44-67).

Jarstad et al (US 6,472,723) teaches cleaning a contact hole after etching using a combination of dry cleaning and wet chemical cleaning (col 3, ln 40-50).

Yu (US 5,940,726) teaches residual oxides within a contact opening are removed by wet or dry cleaning techniques or a combination of the two (col 2, ln 50-60).

Kawai (JP 2000-100749) is a 102(b) equivalent to US 6,284,664.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew J Song whose telephone number is 703-305-4953. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin L Utech can be reached on 703-308-3868. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9310 for regular communications and 703-872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

Matthew J Song
Examiner
Art Unit 1765

MJS
July 28, 2003

BENJAMIN L. UTECH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700